AMENDMENTS TO THE CLAIMS:

Claim 1-17 (canceled)

18. (new) A stack management system for a computer system for executing operations involved in stack-based instructions out of order, comprising:

a register file having entries, each of which can hold a word of data;

an advanced pointer stack that having entries, each of which can hold an entry address in said register file, and, in combination with said register file, is adapted to virtually configure the operand stack depending on all the issued instructions;

a completed pointer stack having entries, each of which can hold an entry address in said register file, and, in combination with said register file, is adapted to virtually configure the operand stack depending on all the completed instructions;

a data buffer constructed as a circular buffer having entries, each of which can hold a word of data; and

a data cache, wherein:

spill/fill operations can be performed between said register file and said data buffer and said data cache.

19. (new) A stack management system for a computer system for executing operations involved in stack-based instructions out of order, comprising:

a register file having entries, each of which can hold a word of data;

an advanced pointer stack having entries, each of which can hold an

entry address in said register file, and, in combination with said register file, is adapted to virtually configure the operand stack/ uppermost part of the operand stack depending on all the issued instructions;

a completed pointer stack having entries, each of which can hold an entry address in said register file, and, in combination with said register file, is adapted to virtually configure the operand stack/ uppermost part of the operand stack depending on all the completed instructions;

a data buffer constructed as a circular buffer having entries, each of which can hold a word of data, and being able to hold the common remaining lower part of said two operand stacks; and

a data cache, wherein:

spill/fill operations can be performed between said register file and said data buffer and between said data buffer and said data cache.